

CSE 460

VLSI LAB

ASSIGNMENT 05

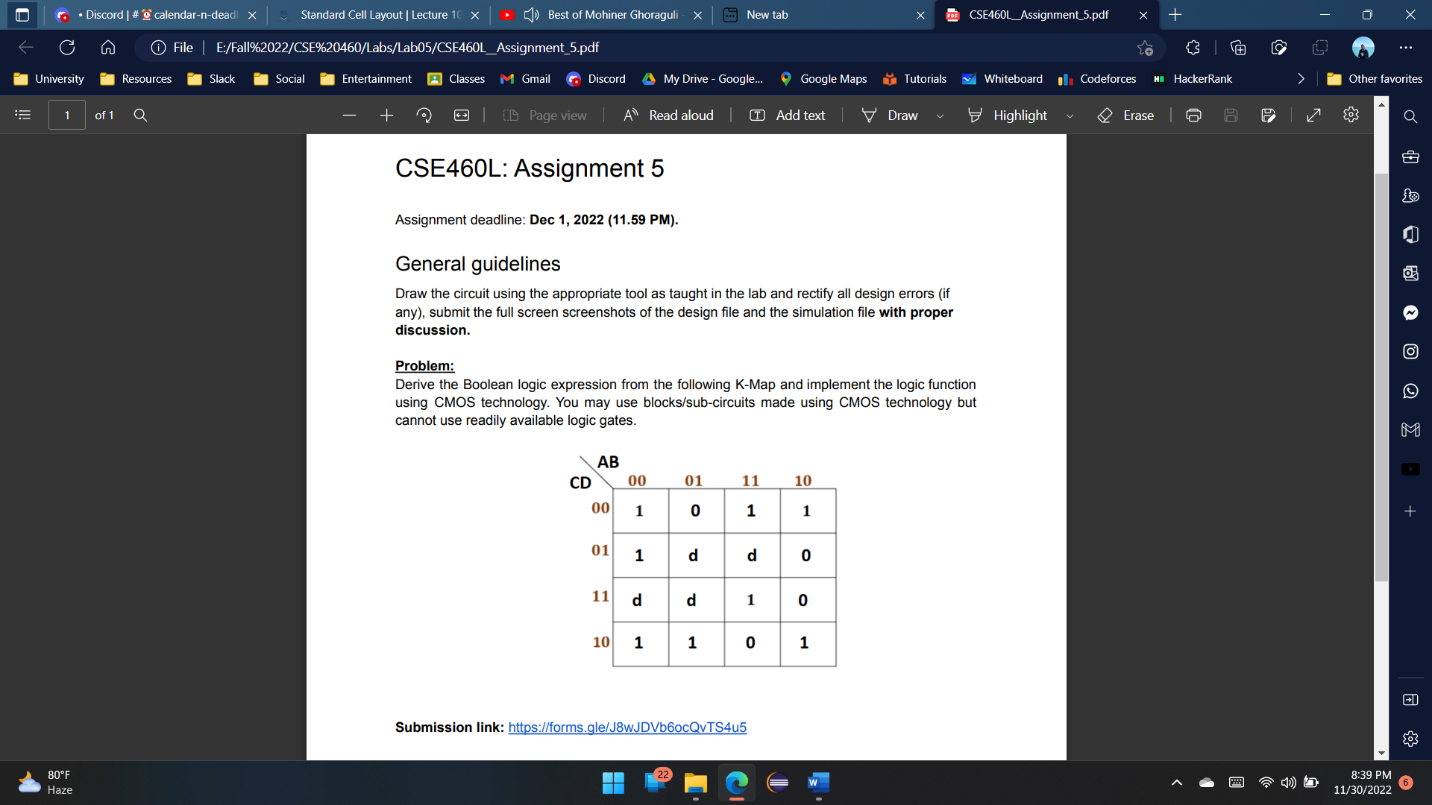
**Submitted by**

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CSE-460 Fall-2022

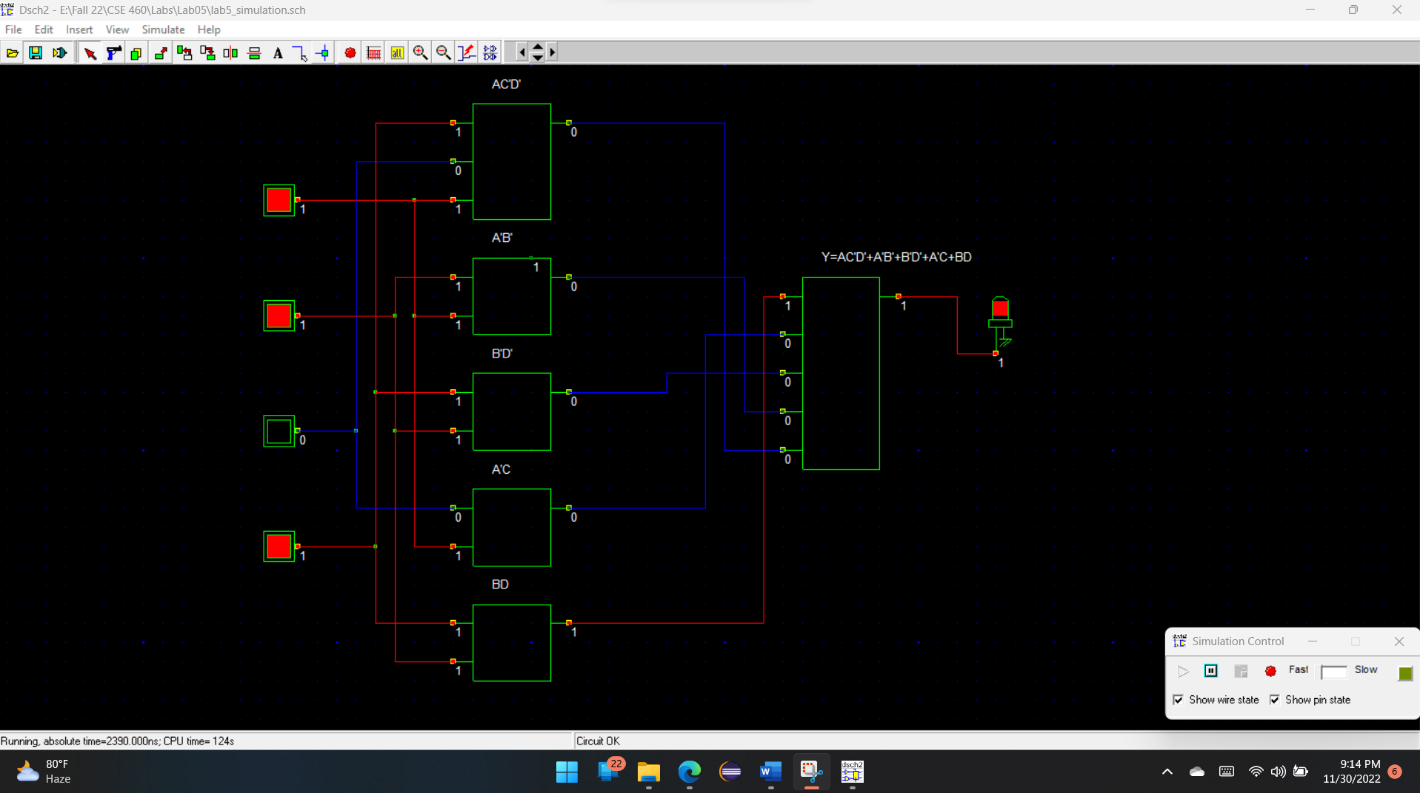
Submission Date: 30th November 2022

**Lab Assignment 05**

**Problem statement**

**Diagram

Description automatically generatedDiagram**

**Simulation**

**Timing Diagram**

**Graphical user interface, application, table, Excel

Description automatically generated**

**Discussion**

From the timing diagram if we compare it with the truth table, we can find that in between 2000ns-3000ns when A, B, C, D are low we get the output high. Also, when A is high and B, C, D are low we get high output at Y. Then again, when A, B, C are low, and D is high we get a high output at Y. Now if we look in between 4000ns to 5000ns, when our input A is low, B is high and other two inputs are low then we get a low output at Y. So, our timing diagram is completely representing the truth we’ve got.